The Influence of Power Chip's Neutron Radiation Effect on Nanometer SRAM's Data Status

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Abstract

This paper compares the differences of neutron radiation effect when SRAM is powered by power chip or DC power. The experiment result shows that before the neutron fluence reaches up to 9.2×10^{12} cm^{-2}, the main factor that causing SRAM upset is neutron induced single event effect whether SRAMs are powered by power chip or DC power. When the total neutron fluence is beyond 9.2×10^{12} cm^{-2}, the power chip can't function well and output regularly and then the SRAM which is powered by power chip will upset drastically due to the breakdown of supply voltage. This is because of the displacement damage of power chip caused by neutrons. However, for SRAM which is powered by DC power, even though the total neutron fluence is beyond 9.2×10^{12} cm^{-2}, neutron induced single event effect is still the main reason that causing it upset.

Keywords: Displacement damage; neutron induced single event effect; power chip; DC power supply; SRAM

1. Introduction

With the development of semiconductor technology, the semiconductor device has higher integration level, better performance and lower power dissipation. SRAM (SRAM: Static Random Access Memory) is widely used in electronic systems as cache due to its fast access speed. It can be used in digital processing device, information processing device and automatic control equipment. SRAM lost its all data when the power breakdown as SRAM is volatile memory. Hence, to investigate the influence of power chip's neutron radiation effect on SRAM's data status is of great important. When SRAM work in neutron radiation environment, its function will be influenced by the neutron radiation effect[1-3].

To investigate the difference of neutron radiation effect when the SRAM powered by DC power or power chip, we divided SRAMs into two groups that one group is powered by power chip and the other is powered by DC power. After neutron irradiation experiment, we obtained the failure mode of two groups of SRAMs that corresponds to two different neutron radiation effects. The difference and the mechanism of two neutron radiation effects are analyzed.

2. Experimental details

To investigate the neutron radiation effect of two groups of SRAMs, we carried out experiment using Xi'an pulse reactor (XAPR). During experiment, the operated power of XAPR is 500 kW with the neutron flux is 2.67×10^{10} $cm^{-2}\cdot s^{-1}$ and the neutron/gamma ray ratio (n/γ ratio) is 7.7×10^{9} $cm^{-2}\cdot rad(Si)^{-1}$.

The device under test is the 130 nm SRAM designed by ISSI whose type is IS62WV1288DBLL. And its nominal working voltage is from 2.3 V to 3.6 V. Fig.1 shows the functional schematic of IS62WV1288DBLL. A0-A16 are address pins and I/O 0-I/O 7 are data pins. CS1 and CS2 are used to input chip selected signal. OE is used to control output function and WE is used to control read and write functions. Its total capacity is 1 Mbits with 128 K (128×1024) addresses and each addresses has 8 bits.

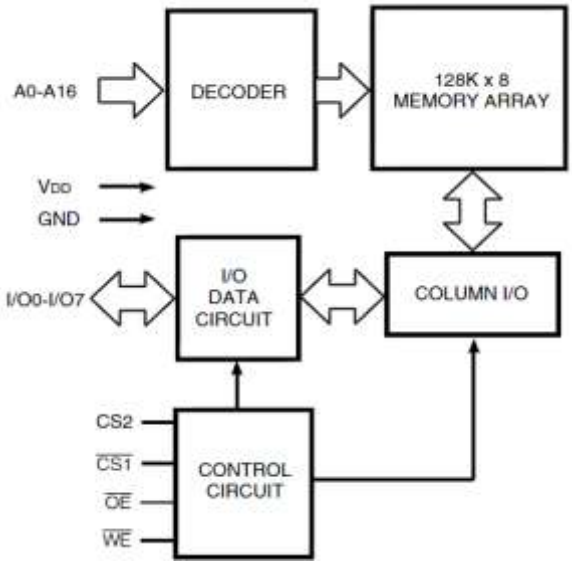


Fig. 1. Functional schematic of IS62WV1288DBLL.

The power chip we choose is designed by TI whose type is LM2576T-3.3. It is a step down power supply management which is monolithic integrated. The input voltage is from 6 V to 40 V, and the output is constant voltage of 3.3 V. It can provide the drive current up to 3A. Fig. 2 shows the functional schematic of LM2576T-3.3. It is integrated with frequency compensation and fixed frequency generator and the switching frequency is 52 kHz.

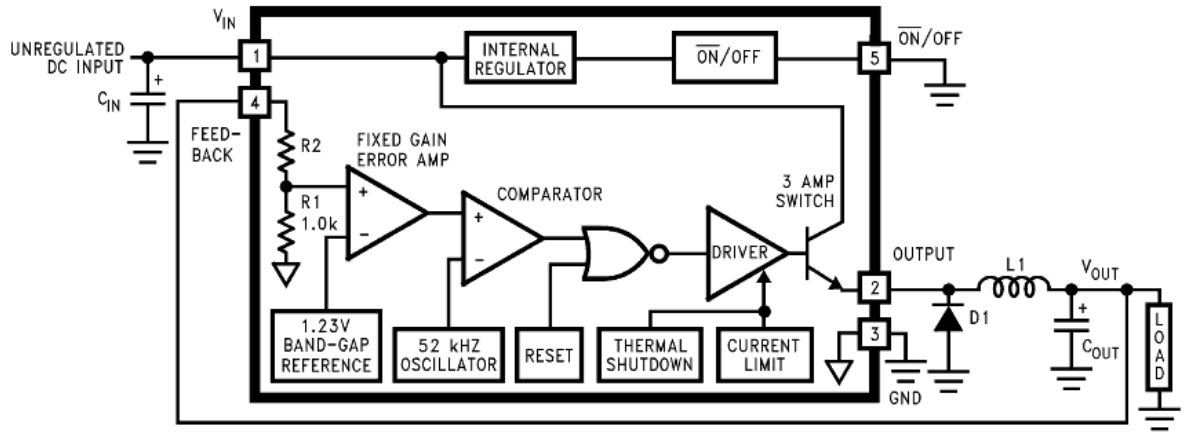


Fig. 2. Functional schematic of LM2576T-3.3.

SRAMs were weld on the irradiation board as its storage data was measured through the connection of test board and irradiation board by flat cable. The irradiation board was designed including four SRAMs (1#, 2#, 3#, 4#) and one power chip which is shown in Fig. 3. SRAMs were divided into two

groups, 1# and 3# were powered with 3.3 V input voltage by power chip and the power chip was powered with 7 V input voltage by DC power. 2# and 4# were powered by DC power through long cable about 20 meters.

During experiment, the orientation of the incident neutrons was vertical with respect to the front surface of the tested SRAMs. All the SRAMs were under static testing. Loading up a uniform byte pattern 55 (hex) before irradiation and then scanning each of them every five seconds for upset errors in sequential logic address during neutron irradiation. For a single scan of each SRAM device, the logic states of all the memory cells in the tested SRAM device were monitored within three seconds for a single scan. The test system compared the data of two read-back cycle dynamically to get the upset status of SRAM.

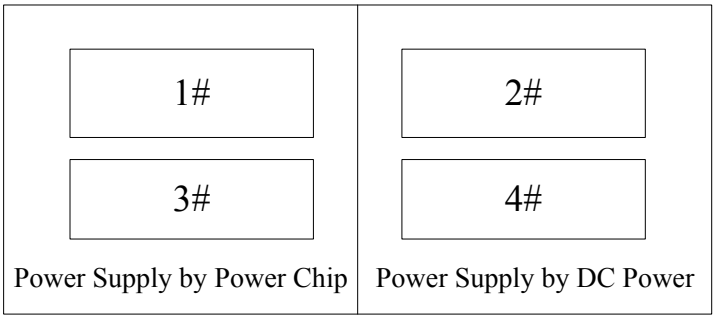


Fig. 3. Schematic diagram of irradiation board.

3. Experimental results and discussion

3.1 The power chip's neutron radiation effect

During neutron radiation experiment, we have monitored the change of power chip's output voiltage. Fig. 4 shows the variation of power chip's output voltage with neutron fluence. With the accumulation of neutron fluence, the output voltage decreased steadily. The output voltage changed from 3.3 V to 3.2 V as the neutron fluence changed from 0 cm^{-2} to 9.2×10^{12} cm^{-2} and the failing range is about 3%. However, when the neutron fluence is beyond 9.2×10^{12} cm^{-2}, the output voltage decreased dramatically. And the output voltage is 0.1 V until the neutron fulence is up to 1.0×10^{13} cm^{-2}. From Fig. 4 we can conclude that there is a threshold of neutron fluence making the power chip fail to work. And the threshold is about 9.2×10^{12} cm^{-2}.

The displacement damage effect was the main reason that causing the power chip failed to work [4]. It is caused by non-ionizing energy deposition which can be called as displacement energy deposition. A large number of displaced atoms are generated in semiconductor material through displacement energy deposited by neutrons. And then results in a large number of defects of all kinds. The degradation of semiconductor device's performance is relative to the number and the types of defects. And the displacement damage effect is permanent. Hence, if the neutron fluence of power chip is up to 9.2×10^{12} cm^{-2}, it can't work normal again.

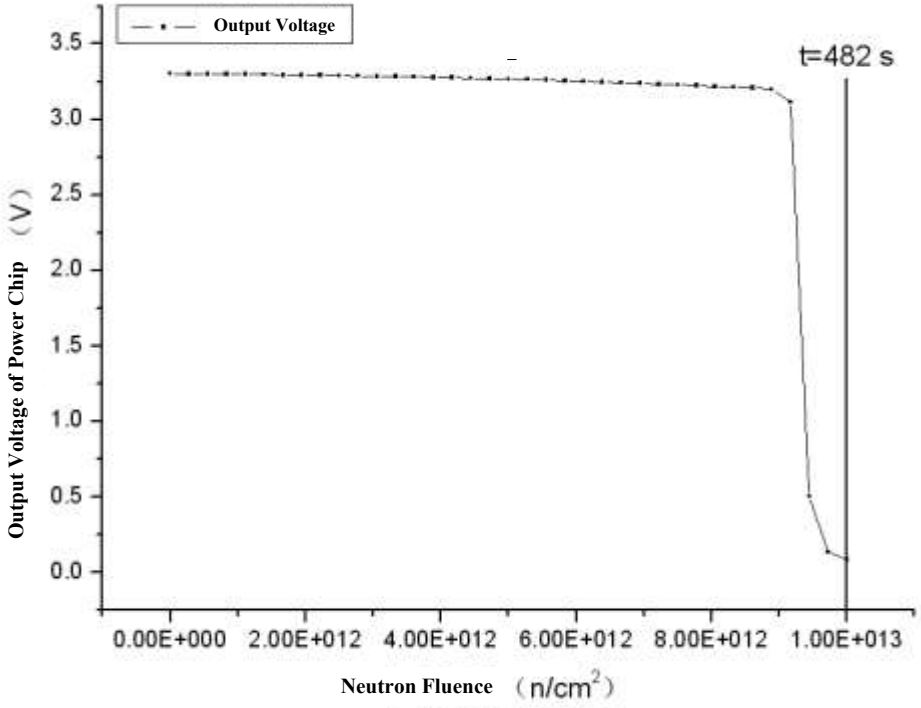


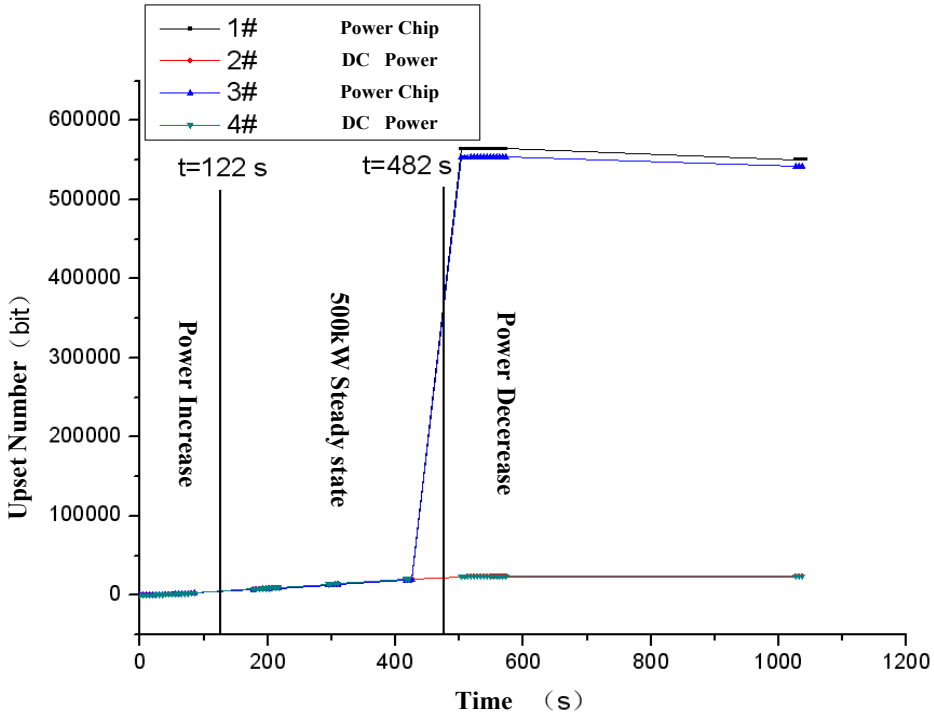
Fig. 4. The variation of power chip's output voltage with neutron fluence.

3.2 The neutron radiation effect of SRAM powered by different power supply

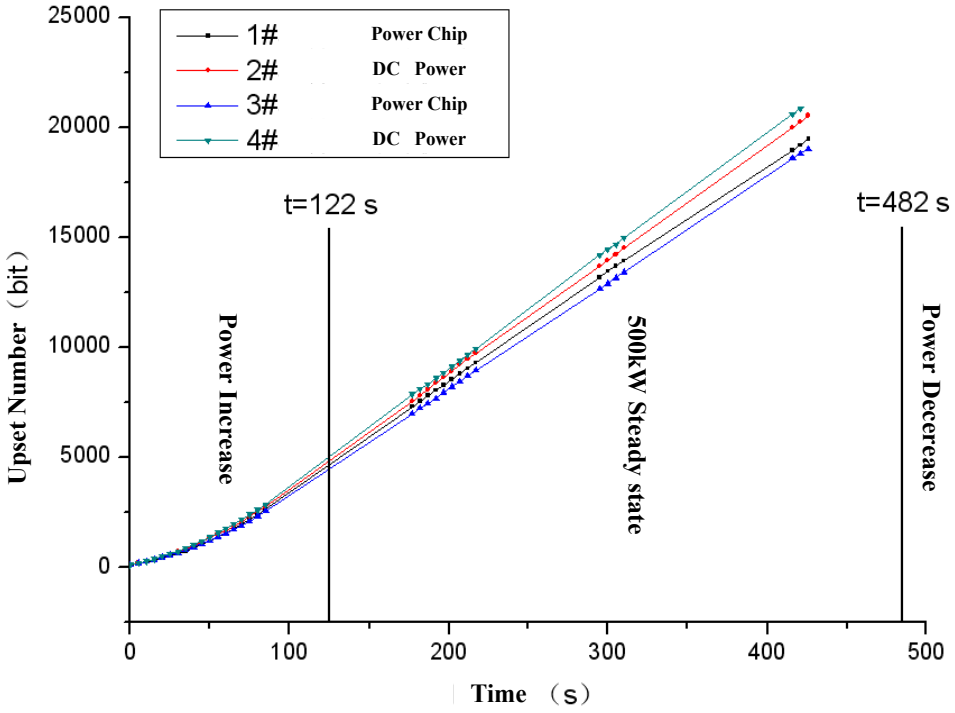
As mentioned before, we divided the SRAM into two groups, one group (1# and 3 # SRAM) were powered by power chip and the other group (2# and 4# SRAM) were powered by DC power as shown in Fig. 3. We test the upset number of SRAM during neutron radiation and the test curve of SRAM's upset number over time (neutron fluence) is shown in Fig. 5. Fig. 5(1) gives the whole process of reactor's operation including power increasing, power decreasing and steady state as Fig. 5(2) just gives the steady state of reactor. From Fig. 5(1) we can see that before the neutron fluence reach to 9.2×10^{12} cm^{-2}, the upset number of all the SRAMs increase linearly with time. When the neutron fluence is beyond 9.2×10^{12} cm^{-2}, the upset numbers of 1# and 3# SRAM which is powered by power chip increase drastically to about 0.5 Mbits. However, the tendency of upset numbers' variation of 2# and 4# SRAM which is powered by DC power does not change.

As 1# and 3# SRAM's maximum upset number is about 0.5 Mbits, it is exactly half of the capacity of IS62WV1288DBLL. Combined with the output voltage of power chip, we can draw the conclusion that the vast upset number was caused by the breakdown of power chip when the neutron fluence is beyond 9.2×10^{12} cm^{-2}, which making the memory cell of SRAM lost its stored information. And during the test process, the data of SRAM's memory cell is random hence the total upset number is half of the total capacity. Therefore, the failure of 1# and 3# SRAM when the neutron fluence is beyond 9.2×10^{12} cm^{-2} is mainly because the displacement damage effect of power chip.

It is shown in Fig. 5(2) that before the neutron fluence reaches to 9.2×10^{12} cm^{-2}. The slope of the upset number verse time increases with the increasing of reactor's power. And when the reactor operated in steady state, the slope does not change again. The upset cross section of SRAMs in



(1)



(2)

Fig. 5. The test curve of SRAM's upset number over time (neutron fluence). (1) The whole process of reactor's operation. (2) Operation of reactor's steady state.

reactor's steady state is equal to the slope of zero-crossing linear fitting of N_{upset}/N_{total} and φ which can be calculated by the formula (1), where N_{total} is memory capacity of the SRAM device. φ is total neutron fluence, and N_{upset} is total upset numbers of SRAM.

$$\sigma = \frac{N_{upset}}{N_{total} \times \varphi} \tag{1}$$

Table 1 shows the upset cross sections of SRAM with different power supply when reactor operates in steady state. The upset cross sections of four SRAMs are very close. The maximum upset cross section and the minimum upset cross section have discrepancy about 9%. We can also see that 2# and 4# SRAM's upset cross section are bigger than 1# and 3# SRAM's upset cross section. That is maybe due to the environment noise feeding in long cable that is used to power 2# and 4# SRAM. As 1# and 3# SRAM are powered by power chip, the output voltage is relatively stable because the input voltage of power chip is ranging from 6 V to 40 V.

Table 1 Upset cross sections of SRAM with different power supply

Power supply mode	Serial Number of SRAM	Upset Cross Section ($cm^{-2} \cdot s^{-1}$)	Upset Number (bits)
Power chip	1#	1.74×10^{-15}	19182
	3#	1.73×10^{-15}	18811
DC power	2#	1.86×10^{-15}	20253
	4#	1.90×10^{-15}	20849

From Fig. 5 we can see that before the neutron fluence reaches to 9.2×10^{12} cm^{-2} when the power chip still can function well, the upset numbers of all the SRAMs increase with time linearly. Therefore, during this time the upset of all the SRAMs are caused by the neutron induced single event effect. The neutron induced single event effect is caused by ionizing energy deposition which is due to the interactions of neutrons with matter and then produce secondary charged particles which can cause atomic ionization during transport[5-6]. The ionizing energy deposition changes the concentration of carriers and the charge states of defects but it is short time and repairable.

Hence, we can see that before the neutron fluence reaches to the failure threshold of power chip, the upset of all the SRAMs is caused by neutron induced single event upset effect. When the neutron reaches to threshold, the power chip can't function well due to displacement damage effect and SRAM will upset drastically. However, if the SRAM is powered by DC power, the upset of SRAM is caused by the neutron induced single event upset as the upset number increases with time linearly.

4. Conclusion

From the experiment results, we can see that when a system consisting of a power chip and a SRAM chip irradiated by the neutron of the reactor, the power chip's output voltage will decrease and can't function well when the neutron fluence reaches up to 9.2×10^{12} cm^{-2}. And then the SRAM devices

which is powered by the power chip lost its all data. Hence, the displacement damage effect of power chip when the neutron fluence of reactor reaches the failure threshold caused the loss of SRAM's data as the upset number have a spurt growth. When the SRAM was powered by the DC power, the main reason caused SRAM upset is neutron induced single event effect, the upset number caused by this factor is growing linearly with time. Hence, the power supply has an important impact on the radiation effect electronic system.

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